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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/991,277	11/09/2001	Donald M. Bartlett	LSI.08USC1 (95-133/1P/1C/	3839

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LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/991,277	BARTLETT ET AL.	
	Examiner	Art Unit	
	Ida M Soward	2822	

-- The MAILING DATE of this communication appears on th cover sh et with the correspond nce address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Applicants' response filed November 28, 2003.

Drawings

Figure 1 should be designated by a legend such as **--Prior Art--** because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 1 in view of Pruijmboom et al. (US 2002/0030244 A1) and Wu (5,998,277).

Admitted Prior Art Figure 1 teaches an integrated circuit having a plurality of circuits **10** & **30** formed on a common substrate **15** and circuitry formed on predetermined portions of the common substrate. However, Admitted Prior Art Figure 1

fails to teach embedded regions buried in the common substrate and isolation regions. Pruijmboom et al. teach the embedded regions **27** are buried in the common substrate **10**; and boron and phosphorus ions (Figure 10, pages 4-5, paragraphs [0033]-[0044], respectively). Wu teaches isolation regions **14**; masking predetermined locations of a common substrate **2** (Figure 6, col. 4, lines 4-27). In regard to claims 2 and 7, Pruijmboom et al. further teach a common substrate 10 having low doping P- and a first predetermined resistance; circuitry formed on predetermined portions of the common substrate; embedded regions of the common substrate that are implanted with ions such that the embedded regions having a resistance that is lower than the first predetermined resistance, the embedded regions being substantially aligned with the circuitry and buried in the common substrate (Figure 10, pages 4-5, paragraphs [0033]-[0044], respectively). Also in regard to claims 1 and 2 concerning the currents being injected into the common substrate, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). In regard to claims 3 and 8, Pruijmboom et al. teach a common substrate including an epitaxial layer 12 and an underlying substrate layer 10 (Figure 10). In regard to claims 1 and 9-7, Initially, and with respect to claims, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554

does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113. Since Admitted Prior Art Figure 1, Pruijmboom et al. and Wu are from the same field of endeavor (integrated circuits), the purpose disclosed by Wu would have been recognized in the pertinent art of Admitted Prior Art Figure 1 and Pruijmboom et al. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Admitted Prior Art Figure 1 by incorporating the embedded regions of Pruijmboom et al. and the isolation region of Wu to recover implant-induced damage (abstract).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure, Pruijmboom et al. (US 2002/0030244 A1) and Wu (5,998,277) as applied to claims 1-3 and 5-11 above, and further in view of Rumennik et al. (US 2002/0050613 A1).

Admitted Prior Art Figure, Pruijmboom et al. and Wu teach all mentioned in the rejection above. However, Admitted Prior Art Figure, Pruijmboom et al. and Wu fail to

teach embedded regions formed in a checkerboard pattern. Rumennik et al. teach embedded regions formed in a checkerboard pattern (page 4, paragraph [0058]). Since Admitted Prior Art Figure 1, Pruijmboom et al., Wu and Rumennik et al. are from the same field of endeavor (integrated circuits), the purpose disclosed by Rumennik et al. would have been recognized in the pertinent art of Admitted Prior Art Figure 1, Pruijmboom et al. and Wu. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Admitted Prior Art Figure 1, the embedded regions of Pruijmboom et al. and the isolation region of Wu with the checkerboard pattern embedded regions of Rumennik et al. to take advantage of multi-dimensional depletions (page 4, paragraph [0058]).

Response to Arguments

In regard to Admitted Prior Art Figure 1, Figure 1 is described as being the background of the invention.

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respects to integrated circuit structures having isolation in the common substrate:

Brown et al. (6,100,143) Gardner et al. (6,111,298)

Huang (US 6,235,593) Sneelal et al. (US 6,391,720 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday, 6:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ims
January 5, 2004